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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/496,793	02/02/2000	Farooq Jabbar	60705-1210	6699

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EXAMINER	
ODOM, CURTIS B	

ART UNIT	PAPER NUMBER
2634	5

DATE MAILED: 10/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/496,793	JABBAR ET AL.	
	Examiner	Art Unit	
	Curtis B. Odom	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1,2,7-10,13,21-24,29 and 30* is/are allowed.

6)☒ Claim(s) *3-6,11,12,14-20 and 25-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 February 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 3, 4, 6, and 27 are rejected under 35 U.S.C. 102(e) as being anticipated by Bedingfield et al. (U.S. Patent No. 6, 236, 675).

Regarding claim 3, Bedingfield et al. discloses a method for timing recovery at the receiver in a DMT communications system (Fig. 5) comprising:

receiving (Fig. 5, element 71, column 1, lines 23-50 and column 5, lines 18-21) a plurality of signals generated and transmitted by an associated far-end transmission unit, wherein the received signal contains multiple signals created by DMT modulation (column 2, lines 2-10);

converting (Fig. 5, block 73, column 5, lines 21-16) the plurality of received signals through an ADC;

detecting (Fig. 5, block 77, column 5, lines 28-39 and 60-61) a phase error between a received pilot tone and a local oscillator signal, wherein the multiplication of the oscillator signal (phase reference signal) and the received pilot tone produce a signal whose DC component is proportional to the phase difference between the incoming pilot tone and the oscillator;

applying (Fig. 5, block 87, column 5, lines 36-40) the phase error to a phase locked-loop to generate a frequency correction signal; and

using (Fig. 5, block 94, column 5, lines 45-62) the frequency correction signal to modify the sampling time of the ADC.

Regarding claim 4, Bedingfield et al. discloses the method of claim 3, wherein the detection of phase error is compensated by an offset based on the received signal segment in the initialization sequence (column 5, lines 36-40), wherein scaling and adding the offset compensates the phase error based on the received signal segment (received pilot tone).

Regarding claim 6, Bedingfield et al. discloses a method of claim 3, further comprising synchronizing a DAC in the transmitting path by using a sampling clock derived from the PLL controlled ADC (column 5, lines 52-59), wherein the transmitting path includes a DAC (Fig. 4, block 54).

Regarding claim 27, Bedingfield et al. discloses system for timing recovery at the receiver in a DMT communications system (Fig. 5) comprising:

means for receiving (Fig. 5, element 71, column 1, lines 23-50 and column 5, lines 18-21) a pilot tone generated and transmitted by an associated far-end transmission unit;

means for converting (Fig. 5, block 73, column 5, lines 21-16) the received pilot tone along with other received signals from an analog to a digital signal;

means for detecting (Fig. 5, block 77, column 5, lines 28-39 and 60-61) a phase error between the received pilot tone and a local oscillator signal, wherein the multiplication of the oscillator signal (phase reference signal) and the received pilot tone produce a signal whose DC

component is proportional to the phase difference between the incoming pilot tone and the oscillator;

means for applying (Fig. 5, block 87, column 5, lines 36-40) the phase error to a phase locked-loop to generate responsive to when the cyclic prefix is not present in the digital signal; and

means for using (Fig. 5, block 94, column 5, lines 45-62) the output signal to modify the ADC timing.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bedingfield et al. (U.S. Patent No. 6, 236, 675).

Regarding claim 5, which inherits the limitations of claim 3, Bedingfield et al. further discloses detecting phase error and phase error compensation is performed using a multiplier and a PLL (Fig. 5, block 77, column 5, lines 28-39 and 60-61). Bedingfield et al. does not disclose this task is accomplished by a state machine. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made that since the state machine is also used for phase detection that it could have been implemented in place of the multiplier. Thus, a

state machine used for phase detection is deemed a design choice and does not constitute patentability.

5. Claims 11, 12, 14-20, 25, 26, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aslanis et al. (previously cited in Office Action 7/28/03).

Regarding claim 11, Aslanis et al. discloses a method for timing recovery at the receiver in a DMT communications system (Fig. 1) comprising:

receiving (Fig. 1, block 12, column 3, lines 60-66, column 5, lines 15-16 and 56-60 and column 6, lines 3-12) a standard pilot tone generated and transmitted by an associated far-end transmission unit along with other signal streams at a particular receiver;

converting (Fig. 1, block 32, column 5, lines 15-19) the plurality of received signals through an ADC to create a digital signal stream;

detecting (Fig. 1, block 34, column 5, lines 19-23) the cyclic prefix in the received digital signal stream;

applying (column 6, lines 19-23) the estimated phase error to the input of a PLL to create a frequency correction signal; and

using (column 6, lines 13-27) the frequency correction signal to modify the ADC sampling time.

Aslanis et al. does not disclose using the digital signal stream with the cyclic prefix portion removed to estimate the phase error with a DFT. Aslanis does disclose that the equalized signal stream with the cyclic portion removed is input to a FFT circuit (column 47-31). However, it would have been obvious to one skilled in the art at the time the invention was made that phase error can be estimated by applying a FFT or DFT to a sample. Therefore, it would

have been obvious that phase error could have been estimated at this stage since a FFT was applied to the samples. Thus, using a DFT to estimate phase error does not constitute patentability.

Regarding claim 12, Aslanis et al. discloses the method of claim 11, further comprising synchronizing a DAC in the transmitting path by using a sampling clock derived from the PLL controlled ADC (column 5, lines 46-60).

Regarding claim 14, Aslanis et al. discloses a device configured to compensate for the offset in phase error on a received pilot tone based upon the received signal segment in the DMT system initialization sequence (Fig. 1, block 12, column 6, lines 13-27), wherein it is obvious that by compensating for frequency offset in the sampler and maintaining frequency synchronization by using a phase error signal that phase error is compensated in the receiver with the phase-locked-loop. Aslanis et al does not disclose the device is a DSP.

However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the device into a DSP rather than individual devices to perform each step of the phase compensation because this would save cost in building the device and simplify implementation of the device. Therefore, configuring the device into a DSP does not constitute patentablitiy.

Regarding claim 15, which inherits the limitations of claim 14, Aslanis et al. further discloses the phase error compensation is accomplished with a phase comparator (Fig. 1, block 50, column 6, lines 19-27). Aslanis et al. does not disclose the phase error compensation is accomplished by a state machine. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made that since the state machine is also used for phase

error compensation that it could have been implemented in place of the phase comparator. Thus, a state machine used to compensate for phase error is deemed a design choice and does not constitute patentability.

Regarding claim 16, Aslanis et al discloses a device to detect and zero out the cyclic prefix from a received digital stream when the cyclic prefix is present to create an input to a PLL (Fig. 1, block 12, column 5, lines 19-27), wherein the process of removing the cyclic prefix is equivalent to zeroing out the cyclic prefix. Aslanis et al does not disclose the device is a DSP.

However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the device into a DSP rather than individual devices to perform each step of the detection and zeroing out of the cyclic prefix because this would save cost in building the device and simplify implementation of the device. Therefore, configuring the device into a DSP does not constitute patentablitiy.

Regarding claim 17, which inherits the limitations of claim 16, Aslanis et al. further discloses performing a time-domain equalization on a received digital data stream and creating an input to a PLL when the cyclic prefix is zeroed out from the signal stream (column 5, lines 15-27), wherein the process of removing the cyclic prefix is equivalent to zeroing out the cyclic prefix.

Regarding claim 18, Aslanis et al discloses a device configured to detect and remove the cyclic prefix from a received digital stream when the cyclic prefix is present, the device further configured to first perform a time-domain equalization of the digital signal stream, then to perform a discrete Fourier transform (FFT) on the digital signal stream when the cyclic prefix is not present to create a phase error signal for application at the input to a PLL (Fig. 1, block 12,

column 5, lines 15-31), wherein the phase information signal (element 54) input to the phase comparator created by this process is the phase error signal. Aslanis et al does not disclose the device is a DSP.

However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the device into a DSP rather than individual devices to perform each step of the process because this would save cost in building the device and simplify implementation of the device. Therefore, configuring the device into a DSP does not constitute patentablitiy.

Regarding claim 19, Aslanis et al. discloses a system for timing recovery at the receiver in a DMT communications system (Fig. 1) comprising:

an ADC (Fig. 1, block 32, column 5, lines 15-19); and

a phase locked loop (Fig. 1, blocks 46 and 52, column 5, lines 13-27) in configured to compensate for the phase offset and to apply a control signal to the ADC, wherein the received signal samples are synchronized for further processing at a rate compatible with that of a source transmission.

Aslanis et al. does not disclose a state machine in communication with the ADC configured to determine the phase offset on a pilot tone in a received signal segment. However, Aslanis et al. discloses a phase comparator for determining phase offset on a pilot tone is a received signal segment (Fig. 1, block 50, column 6, lines 23-27). Aslanis et al. does not disclose this task is accomplished by a state machine. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made that since the state machine is also used for phase detection that it could have been implemented in place of the phase

comparator. Thus, a state machine used for phase detection is deemed a design choice and does not constitute patentability.

Regarding claim 20, Aslanis et al. discloses the system of claim 19, further comprising:

a sampling clock (Fig. 1, line 44, column 5, lines 46-60 and column 6, lines 13-17) in communication with the ADC, the sampling clock in further communication with a DAC in an upstream data path for synchronizing data transmitted in an upstream direction to the source.

Regarding claim 25, Aslanis et al. discloses system for timing recovery at the receiver in a DMT communications system (Fig. 1) comprising:

an ADC (Fig. 1, block 32, column 5, lines 15-19) configured to create a digital representation of the received signal;

an equalizer (Fig. 1, block 34, column 5, lines 15-23) in communication with ADC configured to perform a time-domain equalization on the received signal;

a DFT (Fig. 1, block 38, column 5, lines 27-31) in communication with the equalizer, the DFT configured to convert the time-equalized received signal; and

a phase locked loop (Fig. 1, blocks, 46 and 52, column 5, lines 13-27) in communication with the ADC and DFT configured to receive pilot tone phase error estimate and to apply a control signal to the ADC, wherein the received signal sample stream is synchronized for further processing at a rate compatible with that of a source transmission.

Aslanis et al. does not disclose the DFT estimates phase error and a symbol synchronizer in communication with the ADC to remove the cyclic prefix. Aslanis et al. does disclose a buffer in communication with the ADC (Fig. 1, block 36, column 5, lines 23-27) for removal of the cyclic prefix from the received signal. Therefore, it would have been obvious to one skilled

in the art at the time the invention was made that phase error can be estimated by applying a FFT or DFT to a sample. Therefore, it would have been obvious that phase error could have been estimated at this stage since a FFT was applied to the samples. It would have also been obvious that the since the symbol synchronizer is also used to remove the cyclic prefix that the symbol synchronizer could have been implemented in the place of the buffer to perform the same function. Thus, using a symbol synchronizer to remove a cyclic prefix is deemed a design choice and does not constitute patentability; and using a DFT to estimate phase error does not constitute patentability.

Regarding claim 26, Aslanis et al. discloses the system of claim 27, further comprising:

a sampling clock (Fig. 1, line 44, column 5, lines 46-60 and column 6, lines 13-17) in communication with the ADC, the sampling clock in further communication with a DAC in an upstream data path for synchronizing data transmitted in the reversed direction to the far-end transmission unit.

Regarding claim 28, Aslanis et al. discloses system for timing recovery at the receiver in a DMT communications system (Fig. 1) comprising:

means for receiving (Fig. 1, block 12, column 3, lines 60-66, column 5, lines 15-16 and 56-60 and column 6, lines 3-12) a standard pilot tone and far-end signal from an associated far-end transmission;

means for converting (Fig. 1, block 32, column 5, lines 15-19) the plurality of received signals from analog to digital signals;

means for detecting (Fig. 1, block 34, column 5, lines 19-23) the cyclic prefix in the received far-end signal;

means for removing (Fig. 1, block 36, column 5, lines 23-27) the cyclic prefix in the received far-end signal;

means for applying (column 6, lines 19-23) the estimated phase error to the input of a PLL to create a frequency correction signal; and

means for using (column 6, lines 13-27) the frequency correction signal to modify the ADC sampling rate.

Aslanis does not disclose means for estimating the phase error in the pilot tone with a DFT. Aslanis does disclose that the equalized signal stream is input to a FFT circuit (column 47-31). Therefore, it would have been obvious to one skilled in the art at the time the invention was made that phase error can be estimated by applying a FFT or DFT to a sample. Therefore, it would have been obvious that phase error could have been estimated at this stage since a FFT was applied to the samples. Thus, using a DFT to estimate phase error does not constitute patentability.

Allowable Subject Matter

6. Claims 1, 2, 7-10, 13, 21-24, 29 and 30 are allowable over prior art because related references do not disclose generating signal segments REVERB and SEGUE using an initial pattern that minimizes pilot tone phase offsets and a symbol synchronizer of zeroing out a signal stream when a cyclic prefix is present in the signal stream to create a frequency correction signal.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Curtis B. Odom whose telephone number is 703-305-4097. The examiner can normally be reached on Monday- Friday, 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 703-305-4714. The fax phone numbers for the organization where this application or proceeding is assigned are 709-872-9306 for regular communications and 703-872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Curtis Odom
September 29, 2003

STEPHEN CHIN
SUPERVISORY PATENT EXAMINER
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